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Implementation of a Novel Pwm Dc-Dc Converter

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Abstract: *This paper presents the implementation of a soft-switching boost dc-dc converter. Passive soft-switching is employed due to its advantages over the active soft-switching and its ability to reduce switching losses. A Laplace transform-based analysis of the converter circuit was carried out to obtain design information which was already published. A complete circuit of the soft switching PWM dc-dc converter prototype is also presented here. Experimental results obtained from the prototype agree closely with the predicted results and this demonstrates the feasibility of the system.*
Keywords: *dc-dc converter, soft switching, pulse width modulation, boost converter, Laplace transform.*

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I. Introduction

This paper is a follow-up to an already published paper: "A NOVEL SOFT SWITCHING PWM DC-DC CONVERTER". In the published paper a Laplace transform-based analysis of the dc-dc converter was carried out to obtain design information. Here the design information is taken some steps further to derive the values of different parameters in a typical soft switching pulse width modulated DC-DC converter.

Semiconductor device switching at high frequency is a major contributor to power loss in converters. Switching devices absorb power when they turn on or off if they go through a transition when both voltage and current are non-zero. As the switching frequency increases, these transitions occur more often and the power loss in the device increases. High switching frequencies are otherwise desirable because of the reduced size of filter components and transformers which reduce the size and weight of the converter circuits.

In resonant switching circuits, switching takes place when the switching device voltage and/or current are/is zero, thus avoiding simultaneous transitions of voltage and current and thereby eliminating switching losses. This type of switching is called "soft" switching. Resonant converters include resonant switch-mode converters, load resonant converters, and resonant dc link converters [1].

A successful soft-switching scheme should be able to reduce the switching losses, diode reverse recovery losses, and switching voltage and current stresses on converter components. Any of the two main soft switching approaches which include the zero-current switching and the zero-voltage switching may be employed depending on the semiconductor device
technology that will be used. For example, MOSFETs present better performance under zero-voltage

switching (ZVS). This is because under zero-current switching the capacitive turn-on losses increase the switching losses and the electromagnetic interference (EMI). On the other hand, insulated gate bipolar transistor (IGBTs) and bipolar junction transistors (BJTs) present better results under zero- current switching (ZCS) which can avoid the turn-off losses caused by the tail current [2].

Furthermore, the last twenty years have witnessed an intensive research with the sole aim of achieving lossless switching of semiconductor devices. Lossless
switching increases circuit efficiency and makes high frequency operation possible thereby reducing the
size and weight of circuit components. Several dc-dc converter configurations aimed at achieving a percentage degree of this goal have been proposed [3,4,5,6,7,8,9]. Each of these proposed circuit topologies has at least one of the following limitations:

(a) Too many circuit components, thus degrading circuit reliability,
(b) High current/voltage stresses on the circuit components,
(c) Complex control circuitry which may include switching current/voltage level detection circuits,
(d) Parasitic capacitor turn-on loss of some of the circuit switches,
(e) Limitation of the output voltage control range to allow for switching transients.

In this paper, a detailed study of the single stage dc-dc employing a versatile and efficient soft-switching circuit cell is presented. In the presented converter, the turn-off and the turn-on of the main active switch and the corresponding freewheeling diode take place under zero-current and/or zero-voltage switching. Also, the turn-on and the turn-off of the circuit cell semiconductor devices take place under zero-current and/or zero-voltage switching. A lossless switching is achieved under the above scheme while the voltage and current

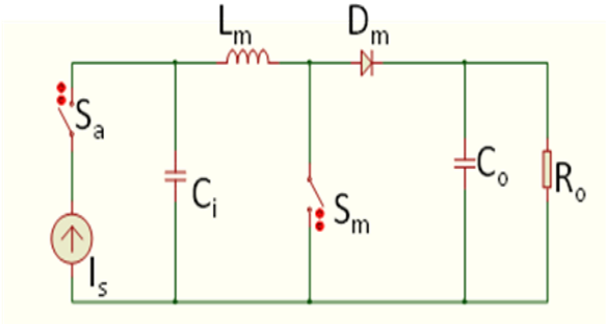
stresses are drastically reduced to the barest minimum through clamping techniques. Figure 1 shows a schematic block diagram of a conventional dc-dc converter.

II. Active/Passive Soft Switching

Higher switching frequencies allow reduction of the magnetic component sizes with pulse width modulated (PWM) switching converters. Unfortunately, increased switching frequencies cause higher switching losses and greater electro-magnetic interference (EMI). The switching loss mechanisms include the current and voltage overlap loss during the switching interval and the capacitance loss during turn-on. The diode reverse recovery also causes an additional conduction loss and further contributes to the current and voltage overlap loss. Soft switched pulse width modulated converters can either be passively soft switched or actively soft switched. Active or passive soft-switching methods have been used to reduce these switching losses.

Recently, passive soft switching has received renewed inspection as a better alternative to active methods. Passive methods do not require an extra switch or additional control circuitry. They are less expensive, have higher reliability and have been reported to achieve higher performance/price ratios than active methods [10, 11]. For PWM converters, passive soft switching reduces switching losses by lowering the active switch's di/dt and dv/dt to achieve zero-current turn-on and zero-voltage turn off. Furthermore, by controlling the di/dt of the active switch, the reverse recovery currents of the diodes are also controlled. The only loss mechanism not recovered with the passive techniques is the energy in the internal capacitance of the switch. However, this loss is much smaller than the other switching losses and may be smaller than the loss incurred by using an auxiliary switch in an active method [10, 11]. Historically, passive soft switching techniques were used to reduce spikes in the switching circuits and were lossy by dissipating the recovered switching energy in resistors [12]. But more recently, many lossless and partially lossless techniques have been proposed [10, 13].

The two necessary components that must be added to the circuit to achieve passive zero-current turn on and zero-voltage turn off are a small inductor and a capacitor. The inductor provides zero-current turn on of the active switch and limits the recovery current of the diodes while the capacitor provides zero-voltage turn off of the active switch. However, the topological rules that describe where these components must be placed in the circuit have not been proposed in the literature. Typically the inductor and capacitor have been placed in series and parallel respectively with the active switch. But many other locations are possible and can lower the component count and reduce switch stress. Also additional circuitry accompanying the capacitor and inductor is used to recover their energy to either the load or the input. There are many different proposed circuits to accomplish this. Furthermore, circuitry cells can be constructed that simplify the creation of new soft switching circuits.



S_a = auxiliary switch; I_s = supply current; C_i = input capacitor; C_o = output capacitor; S_m = main switch; R_o = output resistor(load); L_m and D_m are the main inductor and diode respectively.
Figure1: The Hard switched boost converter

III. Continuous Current Mode

A series connection of the stray inductance and d.c. source voltage is equivalent to a constant current source. Hence, the continuous current mode analysis is as shown below. The circuit has a switching period of T. from figure (1), immediately the main active switch is closed the inductor current rises from an initial value of I_{L1} to a final value of I_{L2} the average of which gives the average input current. When the switch turns off at the end of the on period, the energy stored in the inductor is transferred to the load.

The switching waveforms, shown in figure (2), indicate that the output capacitor conducts a positive current only during off period.

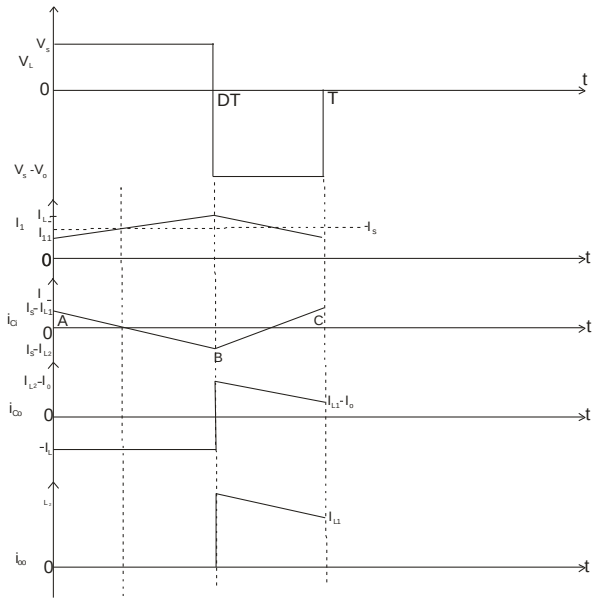


Figure 2: Continuous current switching waveforms

Using average voltage across inductor,

$\frac{1}{T}[\ V_sDT + (V_s - V_o)(1 - D)\ T\ ] = 0$

$V_s\,D + V_s\,(1- D) - V_o\,(1 - D) = 0$

$V_s - V_o\,(1- D) = 0$

$$\frac{Vo}{Vs} = \frac{1}{1-D} \quad \ldots\ldots\ldots\ldots\ldots 1$$

From equation (1), the variation of the duty cycle D gives different values of output voltage with a value tending to infinity as D tends to 1. Also, the average inductor current (I_s) can be the mean of the maximum and minimum value as follows:

$$I_s = \frac{\frac{1}{2}(I_{L1} + I_{L2})DT + \frac{1}{2}(I_{L1} + I_{L2})(1 - D)T}{T}$$

$$= \frac{1}{2}(I_{L1} + I_{L2}) \quad \ldots\ldots\ldots\ldots\ldots 2$$

$$I_o = \frac{\frac{1}{2}(I_{L1} + I_{L2})(1 - D)T}{T}$$

$$I_o = \frac{1}{2}(I_{L1} + I_{L2})(1 - D) = I_S(1 - D)$$

$$\frac{I_o}{I_s} = 1 - D \quad \ldots\ldots\ldots\ldots 3$$

We can also determine the average of i_{ci} and i_{co} from the switching waveforms

I_{ci} = average of i_{ci} = area of (A + B + C)

$$= \frac{1}{T}[1/2(I_s - I_{L1})\frac{DT}{2} + 1/2(I_{s-} I_{L2})\left\{\frac{(1+D)T}{2} - \frac{DT}{2}\right\} + 1/2(I_s - I_{L1})\{\frac{(1 - D)T}{2}\}$$

I_{ci} should be zero over one complete cycle.

That is,

$$I_{ci} = 0 = \frac{\frac{1}{2}(I_s - I_{L1})\left(\frac{DT}{2} + \frac{(1 - D)T}{2}\right) + \frac{1}{2}(I_s - I_{L2})(\frac{T}{2})}{T}$$

$$= \frac{\frac{1}{2}(I_s - I_{L1})\frac{T}{2} + \frac{1}{2}(I_s - I_{L2})\frac{T}{2}}{T}$$

Simplifying further we have,

$$I_S - I_{L1} + I_S - I_{L2} = 0$$

$$I_s = \frac{1}{2}[I_{L1} + I_{L2}]$$

Similarly, for the average of i_{co}, which should be zero also, we have;

$$I_{co} = \frac{1}{T}[-I_o DT + \int_0^{(1-D)T} (I_{L2} - I_o - \frac{(I_{L2} - I_{L1})}{(1-D)T} tdt)] = 0$$

$$= -I_o D + [(I_{L2} - I_O)t - \frac{(I_{L2} - I_{L1})}{2(1-D)T} t^2]_0^{(1-D)T}$$

$$= -I_o D + (I_{L2} - I_o)(1-D) - \frac{(I_{L2} - I_{L1})}{2}(1-D)$$

$$0 = -I_o D + \frac{(I_{L2} + I_{L1})}{2}(1-D) - I_O + I_O D$$

Therefore,

$$I_O = \frac{(I_{L2} + I_{L1})}{2}(1-D)$$

$$\frac{I_o}{I_s} = (1-D) \quad \text{----------4}$$

Equation (4) is another way of deriving equation (3).

Note $I_S = {}^1/_2 (I_{L2} + I_{L1})$.

The minimum and maximum inductor currents are given by the following two equations (where ΔI_L represents the peak to peak variation of the inductor current).

$$I_{L1} = I_S - \frac{\Delta I_L}{2} \ldots\ldots\ldots\ldots\ldots\ldots\ldots 5 \quad I_{L2} = I_S + \frac{\Delta I_L}{2} \ldots\ldots\ldots\ldots\ldots\ldots\ldots 6$$

$$\text{where } \Delta I_L = \frac{V_S\, DT}{L} = \frac{(V_S - V_o)(1-D)T}{L}$$

$$\text{But } V_S = (1-D)V_o$$

$$\therefore \Delta I_L = \frac{[(1-D)V_o - V_o](1-D)T}{L}$$

$$= -D\frac{(1-D)V_o T}{L}$$

$$= -D\frac{(1-D)V_o}{fL}$$

In magnitude,

$$\frac{\Delta I_L}{2} = D\frac{(1-D)V_o}{fL} \ldots\ldots\ldots\ldots\ldots\ldots 7$$

Again maximum ΔI_L occurs at D = ½

Hence in magnitude,

$$\Delta I_{L_{max}} = \frac{V_o}{4fL}$$

Hence,

$$\frac{\Delta I_{Lmax}}{2} = \frac{V_O}{8fL} \quad ------8$$

From the above equation (8) the maximum and minimum inductor currents then become

$$I_{L1} = I_s - \frac{V_s D}{2fL} = I_s - \frac{D(1-D)V_O}{2fL} \quad ---9$$

$$I_{L2} = I_s + \frac{V_s D}{2fL} = I_s + \frac{D(1-D)V_O}{2fL} \quad ---10$$

For continuous current mode,

$$I_{L1} = I_s - \frac{V_s D}{2fL} = I_s - \frac{D(1-D)V_O}{2fL} \geq 0 \quad ---11$$

otherwise current is discontinuous for $I_{L1} < 0$.

The critical inductance for continuous load current for given D, V_s and I_s is,

$$Lc = \frac{V_S\, D}{2fIs} = \frac{D(1-D)V_o}{2fIs}$$

By power balance the input power is equal to the output power, hence

$$V_S I_S = \frac{V_O^2}{R} = I_O V_O$$

That is, $I_s = \frac{V_O^2}{RV_S} = \frac{I_O V_O}{V_S}$

Also, $Is = \frac{I_0}{I-D}$ as was derived before.

The minimum inductance that will guarantee continuous current (the critical inductance), Lc can therefore be expressed in several forms as:

$$L_C = \frac{V_S D(1-D)}{2fI_O} = \frac{D(1-D)^2 V_O}{2fI_O}$$
$$= \frac{D(1-D)^2 R_O}{2f} ------12$$

In terms of the output quantities note that equations (9), (10), (11) can be stated as,

$I_{L1} = \frac{I_o}{1-D} - \frac{D(1-D)V_o}{2fL}$ …… 13

$I_{L2} = \frac{I_o}{1-D} + \frac{D(1-D)V_o}{2fL}$ …… 14

For continuous current mode,

$I_{L1} = \frac{I_o}{1-D} - \frac{D(1-D)V_o}{2fL} \geq 0$

$\frac{I_o}{1-D} \geq \frac{D(1-D)V_o}{2fL}$

$1 \geq \frac{D(1-D)^2 V_O}{2fLI_o}$

that is, $1 \geq \frac{D(1-D)^2 R_O}{2fL}$ ……..15

Otherwise the current is discontinuous

IV. The Input And Output Capacitors' Voltage Ripples

The peak to peak ripple on C_o can be calculated from the fact that C_o discharges at constant current in the interval DT.

$$\Delta V_{C_o} = \frac{I_O}{C_O} DT = \frac{V_O}{C_O R} DT$$

This peak to peak ripple in per unit of the output voltage is,

$\frac{\Delta V_{Co}}{V_o} = \frac{D}{fRC_o}$ …… 16

Also the voltage on the input capacitor can be calculated from the input capacitor current waveform of fig (2) as follows:

$$\Delta V_{C_i} = \frac{\text{area } (A+C) \text{of } i_{c_i}}{c_i} = \frac{\text{area B of } i_{c_i}}{c_i}$$

$$= \frac{1/2(I_S - I_{L_1})DT/2 + \frac{(I_S - I_{L_1})(1-D)T/2}{2}}{C_i}$$

$$= \frac{{}^1/_2 (I_s - I_{L1})\, {}^T/_2}{Ci}$$

But $I_s - I_{L1} = \frac{V_S D}{2fL}$

$\therefore \Delta V_{C_i} = \frac{V_S DT}{2fLC_i} \times \frac{1}{4} = \frac{V_S D}{8f^2 LC_i}$

The peak ripple voltage on the input capacitor is therefore

$\frac{\Delta v_{c_i}}{2} = \frac{v_s D}{16f^2 Lc_i}$ ------17

In per unit of the supply voltage the peak ripple voltage can be expressed as

$\frac{\Delta V_{C_i}}{V_S} = \frac{D}{8f^2 LC_i}$ ------ 18

Our target is to design a circuit which can give an output voltage of 230 volts from a supply voltage of 48 volts over a load of about 105.8 ohms. Hence the average continuous load current can be calculated as,

$I_0 = \frac{V_0}{Ro} = \frac{230}{105.8} = 2.174A$

Also, recall that from our initial analysis [equation (1)] the transfer function for a continuous current circuit is,

$V_0 = \frac{V_s}{1-D}$

Therefore for a supply voltage of 48 volts and output voltage of 230 volts we have,

$V_0 = \frac{V_s}{1-D}$

$230 = \frac{48}{1-D}$

$230 - 230D = 48$

$\therefore D = \frac{230-48}{230} = 0.79$

From the above calculations, our desired circuit will operate at a duty cycle of about 0.79

Considering equation (12) the critical inductance which is the minimum inductance that will guarantee a continuous current operation is given by

$$L_C = \frac{D(1-D)^2 R_O}{2f} = \frac{0.79(1-0.79)^2 x 105.8}{2x20000} = 92.15\ \mu H$$

Also, assuming an output voltage ripple of less than one percent the output capacitor can be calculated from equation (16) as,

$\frac{\Delta V_{C_O}}{V_O} = \frac{D}{fRC_o} < 1\%$

$\therefore C_0 > \frac{D}{Rf(\frac{\Delta V_{C0}}{V_0})} = \frac{0.79}{105.8x20000x0.01}$

$\therefore C_0 > 37.3\mu F$

$C_0 \approx 40\mu F$

Likewise from equation (18) for a ripple voltage of less than 1% under continuous current mode we can calculate the input capacitor as,

$$C_i > \frac{D}{8f^2 L(\frac{\Delta V_{C_I}}{V_s})}$$

$$C_i > \frac{0.79}{8x(20000)^2 x\, 0.000095 x\, 0.01}$$

$C_i > 260\mu F$

When the d.c source is connected in series with an inductance, it has an equivalence of a constant current source. The a.c equivalence can be drawn as follows,

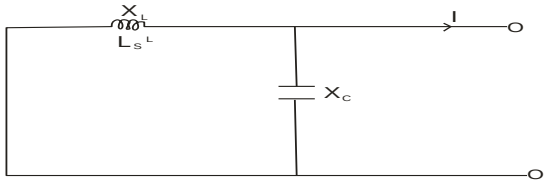


Figure 3: ac equivalent circuit

$\frac{\Delta I_L}{2} = \frac{V_O}{8fL} = I$

The peak current flowing through the stray inductance is expected to be less than 1%

Hence,

$\frac{-jX_c}{j(X_L - X_C)} x\ I < 0.01$

Considering the magnitude,

$\frac{X_c}{X_L - X_c} \leq 0.01$

$\therefore 100\, X_C = X_L - X_c$

$101 X_c = X_L$

But $X_c = \frac{1}{2\pi f C_i}$

Assuming $C_i = 100\ \mu F$

$X_L = 2\pi f L_s$

$$\therefore \frac{101}{2\pi x 20000 x 100\, x 10^{-6}} = 2\pi x 20000 L_S$$

$8.037 = 125663.7\ L_s$

$$\therefore\ L_S = \frac{8.037}{125663.7} = 64\mu H$$

The stray inductance can be arbitrarily chosen to be 100µH.

The design of the soft-switching converter proceeds as follows: immediately auxiliary switch S_a in figure (1) is closed the current flow is the same as that shown in figure below, giving an output current of;

$$I_0 = \frac{P_0}{V_0} = \frac{500}{230} = 2.174A$$

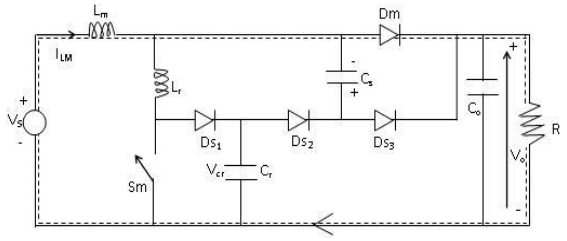


Figure 4: circuit operation after closing S_a

Let L_m = 200µH for continuous load current. The supply current can be calculated from equation (4) as,

$$I_s = \frac{2.174}{1-0.79} = 10.35A$$

This is average value of $i_{Lm.}$ The peak to peak current variation is:

$$\Delta I_L = \frac{V_S D}{2fL} = \frac{48\ x\ 0.79}{2\ x\ 20000\ x\ 200\ x\ 10^{-6}}$$

$$= \frac{48\ x\ 0.79}{8}$$

$$= 4.74\ A$$

$$\therefore\ I_{L_1} = 10.35 - 4.74 = 5.61\ A$$

$$I_{L_2} = 10.35 + 4.74 = 15.09\ A$$

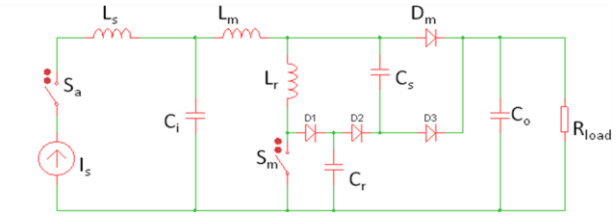


Figure 5: Soft switching dc-dc converter circuit model

V. Conclusion

The compl The soft switching dc-dc pulse width modulation converter designed and implemented is as shown in figure 5 above. The parameter values are as gotten using Laplace-transformed design expressions. The circuit was implemented and was used to light a 230 volts rated bulb.

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